Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 4: Memory Views

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Notices and Disclaimers

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Graphics Memory Address Spaces

The *Graphics Memory Address Spaces* table lists the five supported Graphics Memory Address Spaces. Note that the Graphics Memory Range Removal function is automatically performed to transform system addresses to internal, zero-based Graphics Addresses.

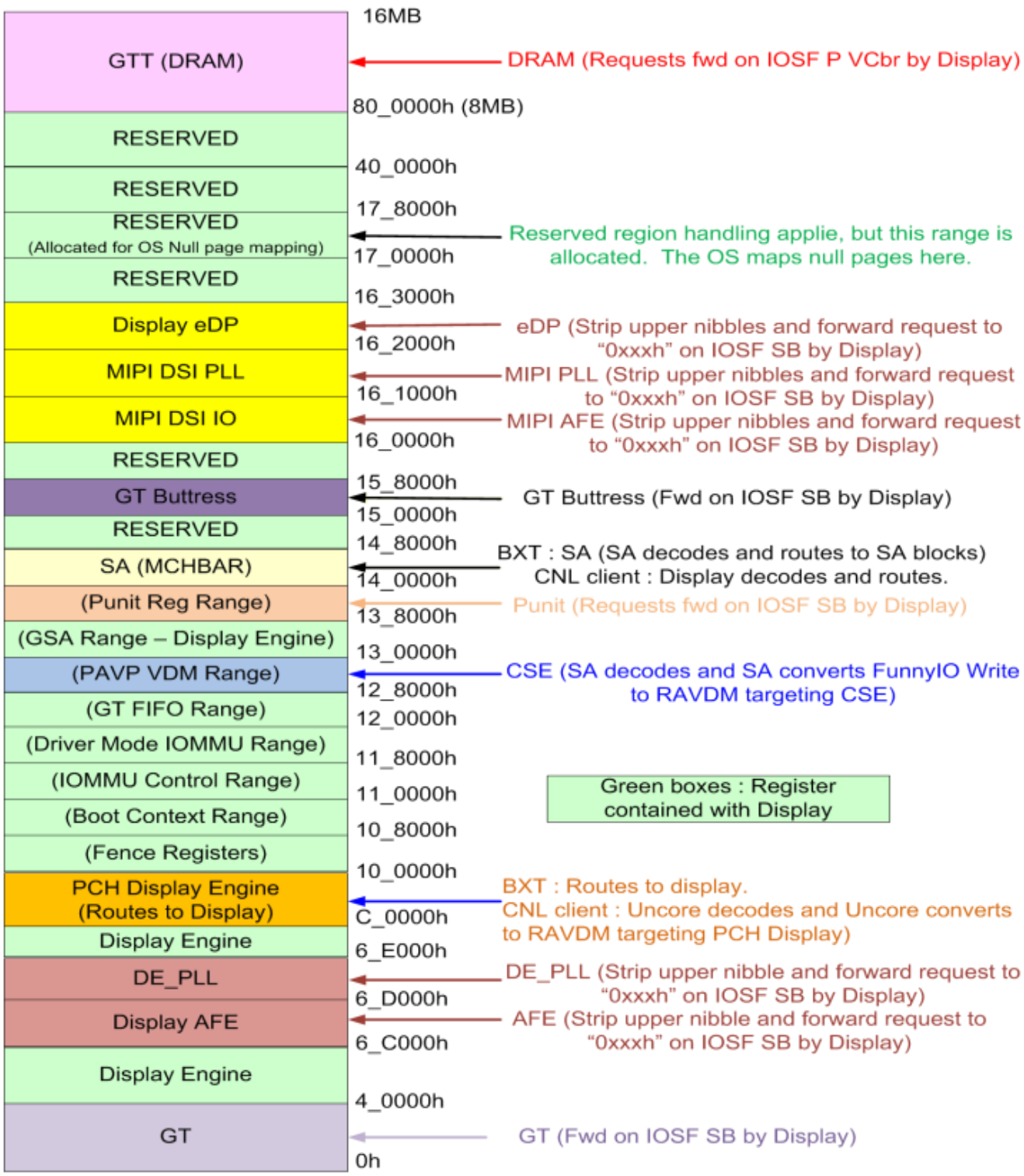
Graphics Memory Address Types

Address Type	Description	Range	Gen9
GMADR	Address range allocated via the Device 2 (integrated graphics device) GMADR register. The processor and other peer (DMI) devices utilize this address space to read/write graphics data that resides in Main Memory. This address is internally converted to a GM_Address.	This is a 4 GB bar above physical memory.	128 MB, 256 MB, 512 MB, 1GB, 2GB, 4GB
GTTMMADR	The combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 8MB of that used by MMIO and 8MB used by GTT. GTTADR will begin at GTTMMADR 8MB while the MMIO base address will be the same as GTTMMADR. For the Global GTT, this range is defined as a memory bar in graphics device config space. It is an alias into which software is required to write Page Table Entry values PTEs. Software may read PTE values from the global Graphics Translation Table GTT. PTEs cannot be written directly into the global GTT memory area.	This is a 16MB bar above physical memory.	16 MB (2 MB MMIO + 6 MB reserved + 8 MB GGTT)
GTTMMADR	The MMIO allocation will either be : 2MB MMIO + 6MB reserved..	This is a 16MB bar above physical memory.	16MB (2MB MMIO + 6MB reserved + 8MB GGTT)
GSM	GTT Stolen Memory. It is an 8 MB (max) region taken out of physical memory to store the Global GTT entries for page translations specific to GFX driver use. It is accessible via GTTMMADR from the CPU path however GPU/DE can access the same region directly.	This is an 8 MB region in physical memory not visible to OS.	1 MB, 2 MB, 4 MB, 8 MB

Address Type	Description	Range	Gen9
DSM	Data stolen memory, the size is determined with GMS filed (8 bits) with MAX size of 4 GB. This is a stolen memory which can be accessed via GMADR for CPU and directly for GPU/DE. Size is programmable with 32 MB multiplier. First 4KB of DSM has to be reserved for GFX hardware use.	This is a max of 4 GB stolen physical memory for GFX data structures.	0 MB, 32 MB, 64 MB, 96 MB, ...4096MB
PCM/WOPCM	Reserved within the DSM for protected content functions.	Limited by the DWM size, base is programmable.	

Next level breakdown for GTTMMADR is given below.

Software is allowed to use range x17_0000 to x17_FFFF as the Null range.


GTTMMADR targets
16MB
GTT (DRAM)
DRAM (Requests fwd on IOSF P VCbr by Display)
80_0000h (8MB)
RESERVED
40_0000h
RESERVED
17_8000h
RESERVED
(Allocated for OS Null page mapping)
Reserved region handling applie, but this range is allocated. The OS maps null pages here.
17_0000h
RESERVED
16_3000h
Display eDP
eDP (Strip upper nibbles and forward request to "0xxxh" on IOSF SB by Display)
16_2000h
MIPI DSI PLL
MIPI PLL (Strip upper nibbles and forward request to "0xxxh" on IOSF SB by Display)
16_1000h
MIPI DSI IO
MIPI AFE (Strip upper nibbles and forward request to "0xxxh" on IOSF SB by Display)
16_0000h
RESERVED
15_8000h
GT Buttress
GT Buttress (Fwd on IOSF SB by Display)
15_0000h
RESERVED
14_8000h
SA (MCHBAR)
BXT : SA (SA decodes and routes to SA blocks)
CNL client : Display decodes and routes.
14_0000h
(Punit Reg Range)
Punit (Requests fwd on IOSF SB by Display)
13_8000h
(GSA Range – Display Engine)
13_0000h
(PAVP VDM Range)
CSE (SA decodes and SA converts FunnyIO Write to RAVDM targeting CSE)
12_8000h
(GT FIFO Range)
12_0000h
(Driver Mode IOMMU Range)
11_8000h
(IOMMU Control Range)
11_0000h
Green boxes : Register contained with Display
(Boot Context Range)
10_8000h
(Fence Registers)
10_0000h
PCH Display Engine
(Routes to Display)
BXT : Routes to display.
CNL client : Uncore decodes and Uncore converts to RAVDM targeting PCH Display)
C_0000h
Display Engine
6_E000h
DE_PLL
DE_PLL (Strip upper nibble and forward request to "0xxxh" on IOSF SB by Display)
6_D000h
Display AFE
AFE (Strip upper nibble and forward request to "0xxxh" on IOSF SB by Display)
6_C000h
Display Engine
4_0000h
GT
GT (Fwd on IOSF SB by Display)
0h

TLB – Final Page Entry

The size of the TLBs has been increased over the previous generation and should be targeting using the following list:

- L3 TLB: 768 TLB entries – This is where all HDC, I$, Constant, State, and Sampler streams are stored.
- MFX: 512 TLB entries – All Media streams (split 256/256 between two media engines).
- BLT: 32 entries.
- Z: 512 TLB entries – All depth accesses.
- C: 256 (256 TLB entries) – All color accesses.
- FF: 128 (128 TLB entries) – All FF accesses to memory.
- VLF: 32 (32 TLB entries) – Media surface.
- GAV: 64 (64 TLB entries) – Video enhancement.
- WiDi: 64 (64 TLB entries) – Wireless Display.

All TLB entries are increased to 48b to contain larger address as well as the page attributes attached to it.

The max size of a single TLB is 256 entries, larger quantities have to be handled as set-associative storages. Set associativity will be managed by low order page bits (i.e. address#12, address#13, ...).

Both Color and Z TLBs are designed to process a single memory request per cycle. To achieve a higher throughput where concurrent Color or Z read/write's are used, following register bit needs to be enabled: mmio0x04A30h [31]

The sizes of RCCTLB and ZTLB only have 256 entries.

Since there is a reduced number of TLB entries in BXT, *the recommended TLB entry allocation in BXT is as follows:*

- When TR-TT is enabled
  - ZTLB: STC(64), HiZ(128), RCZ(48), GATR(16)
  - RCCTLB: MSC(128), RCC(112), GATR(16)
- When TR-TT is disabled
  - ZTLB: STC(64), HiZ(128), RCZ(64)

RCCTLB: MSC(128), RCC(128)

The size of the L3 TLB is also different between projects. The default TLB entry alocations are:

- BXT (L3TLB-Gfx **512**): L3(**64**:*0-63*), DC(**80**:*64-143*), TX(**352**:*144-495*), GATR(**16**:*496-511*)
- BXT (L3TLB-GPGPU **512**): L3(**64**:*0-63*), DC(**368**:*64-431*), TX(**80**:*432-511*)

For giving more TLB resources for both DC and TX, the following allocations are recommended.

- BXT (L3TLB-Gfx **512**): L3(**64**:*0-63*), DC(**432**:*64-495*), TX(**432**:*64-495*), GATR(**16**:*496-511*)
- BXT (L3TLB-GPGPU **512**): L3(**64**:*0-63*), DC(**448**:*64-511*), TX(**448**:*64-511*)