Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics

Programmer's Reference Manual

For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform

Volume 13: Memory-mapped Input/Output (MMIO)

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Force Wake Table

Before initiating reads or writes to power domains that may be off, software must issue the proper "force wake" and verify to guarantee that the register is powered. The following table shows the source and target ranges, and which force wake to use:

	Target			
Source	**Uncore**	**GTI/Blit**	**Render**	**Media**
CPU	n/a	Write A188, then Poll 130044 (Move to 0D8A??)	Write 0xA278[15:0], then Poll 0xD84[15:0]	Write 0xA270[15:0], then Poll 0xD88[15:0]
CS	n/a	n/a	n/a	MI_PIPE_SELECT[5] or R_PWR_CLK_STATE[19] (CS/PM handshake internally)
VCS	n/a	n/a	new MI_FORCE_WAKEUP[0]	n/a
BCS	n/a	n/a	new MI_FORCE_WAKEUP[0]	new MI_PIPE_SELECT[5]
VECS	n/a	n/a	new MI_FORCE_WAKEUP[0]	new MI_PIPE_SELECT[5]
Ranges Affected (0x)	00B00-01FFF	All others	02000-026FF 3000-03FFF 05200-07FFF 08300-084FF 08C00-08CFF 09400-097FF (*) 0B000-0B47F 0E000-0E8FF 24400-245FF 24600-247FF 8140-814C 8150-815C 94D0-951C 9520-956C	08800-089FF 09400-097FF (*) 0D000-0D7FF 12000-13FFF 1A000-1E9FF 30000-3FFFF 8130-813C 9480-94CC

* Note: Some CP registers (0x9400-0x97FF) are replicated in all domains, thus both render and media domains must be awake.

Slice Registers and Die Recovery

When slice 0 is disabled (for example, GT3 fused to GT2 with a slice 0 fault), any read to a slice-located MMIO register must be directed to slice 1, otherwise data of '0' will be returned. This applies to SRM cycles from any command streamer.

MMIO Range Start	MMIO Range End	Unit Description
00005500	00005FFF	WMBE
00007000	00007FFF	SVL
00009400	000097FF	CP unit reg. file - Copy in Slice Common (in all slices)
0000B000	0000B0FF	L3 unique status registers for each slice (unicast per GT).
0000B100	0000B3FF	L3 bank config space (multicast copy per bank and slice)
0000E000	0000E0FF	DM
0000E100	0000E1FF	SC
0000E200	0000E3FF	GWL (inst. 0)
0000E200	0000E3FF	GWL (inst. 1)
0000E200	0000E3FF	GWL (inst. 2)
0000E400	0000E7FF	TDL

SW Virtualization Reserved MMIO range

The MMIO address range from 0x178000 thru 0x178FFF is reserved for communication between a VMM and the GPU Driver executing on a Virtual Machine.

HW does not actually implement anything within this range. Instead, in a SW Virtualized environment, if a VM driver issues a read to this MMIO address range, the VMM will trap that access, and provide whatever data it wishes to pass to the VM driver. In a non-SW-Virtualizated environment (including an SR-IOV Virtualized environment), reads will return zeros, like any other unimplemented MMIO address. Writes to this range are always ignored.

It is important that no "real" HW MMIO register be defined within this range, as it would be inaccessable in a SW-virtualized environment.